**Digital System Design Lab**

**LAB # 07**



Submitted by: Maaz Habib

Registration No: 20PWCSE1952

Class Section: **C**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Submitted to:

**Eng:Muhammad Usman**

**Department of Computer Systems Engineering**

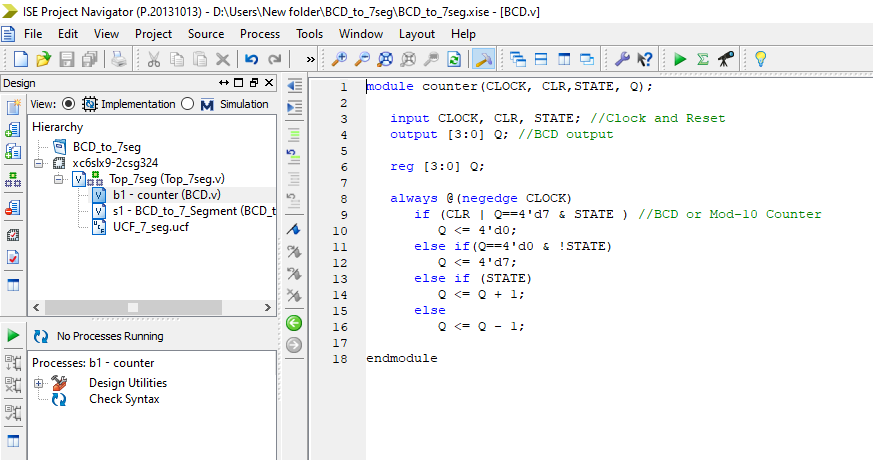
**University of Engineering and Technology, Peshawar**

**Lab # 07**

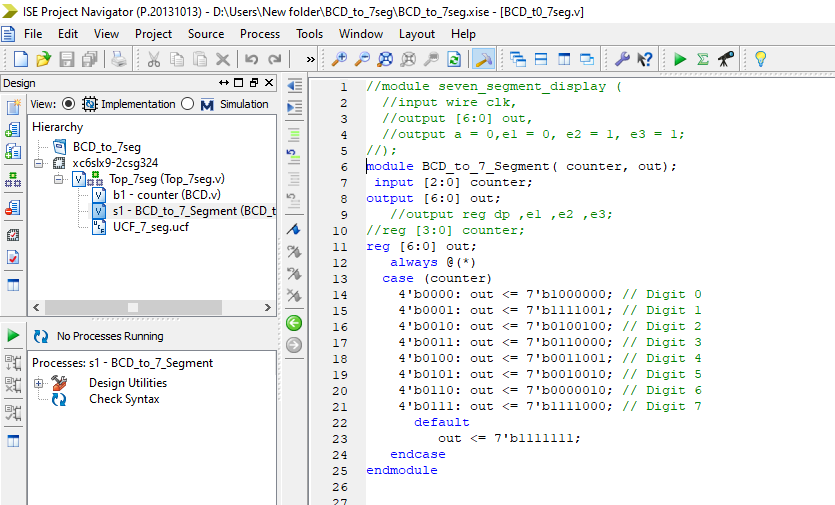
**a.** Desgin/Implementing a 3-bit Up/Down Counter and Displaying the Output Count on LEDs **b.** Desgin/Implementing a 3-bit Up/Down Counter and Displaying the Output Count on a Seven Segment Display

TASK1:

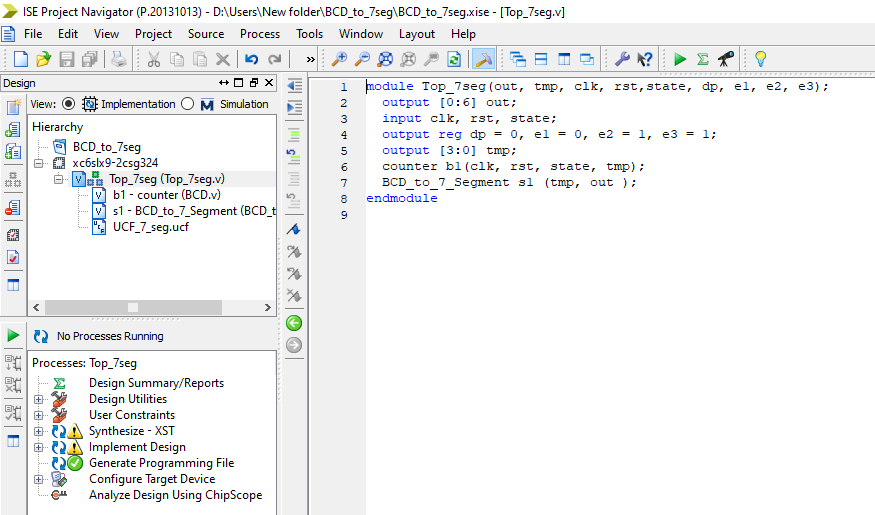
COUNTER

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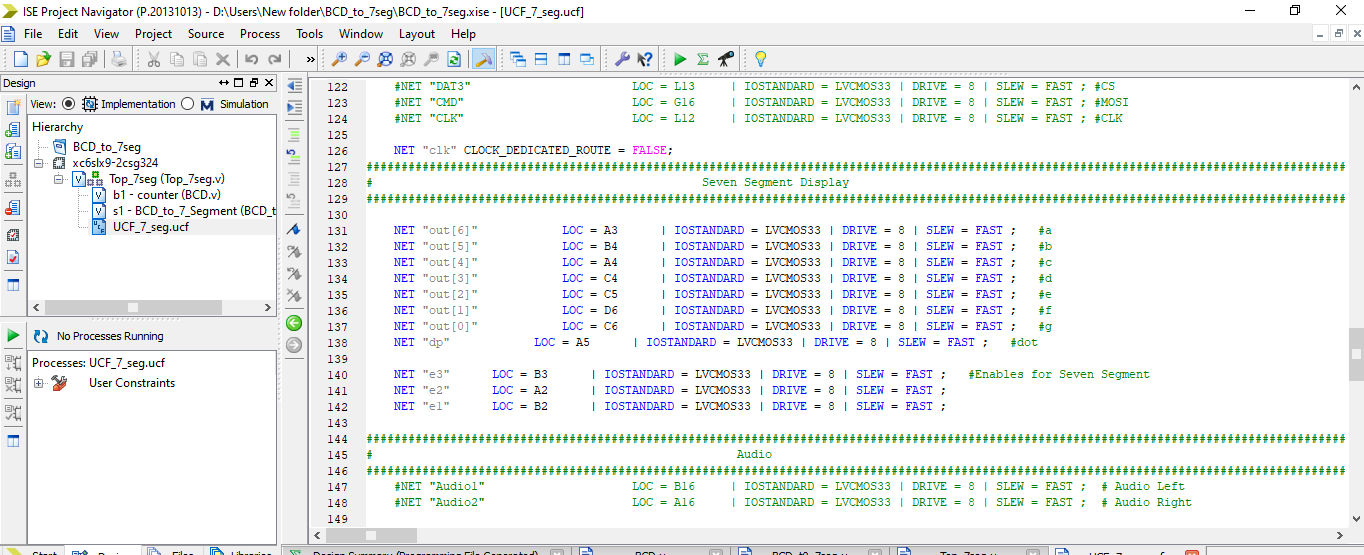
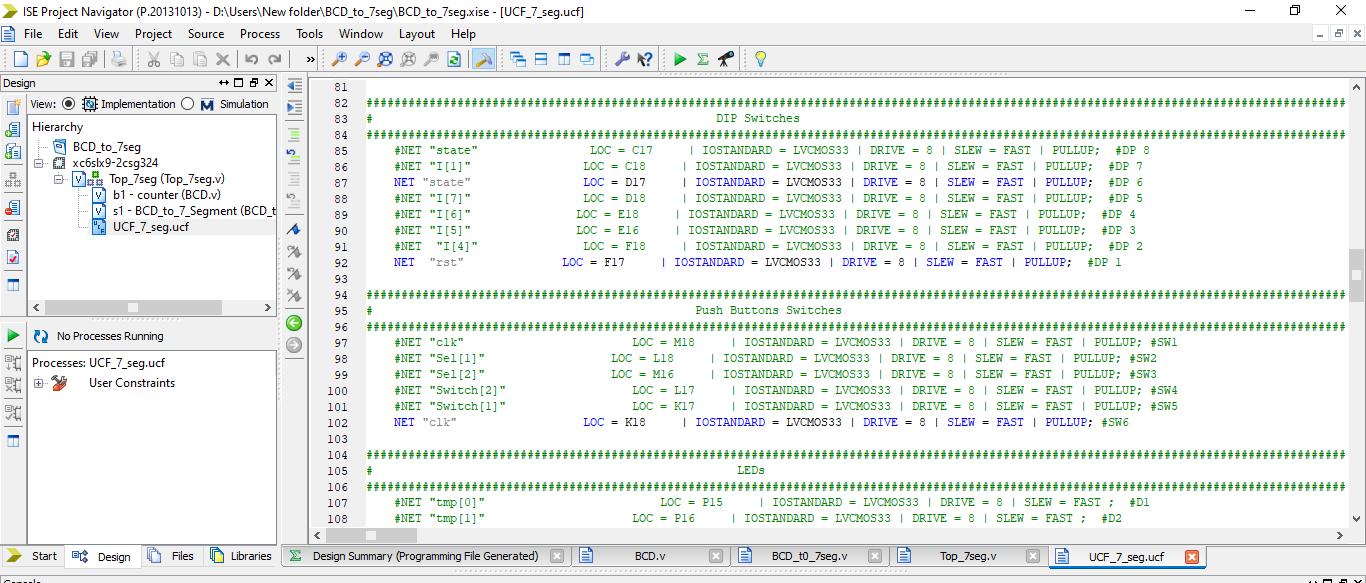
BCD TO SEVEN SEGMENT

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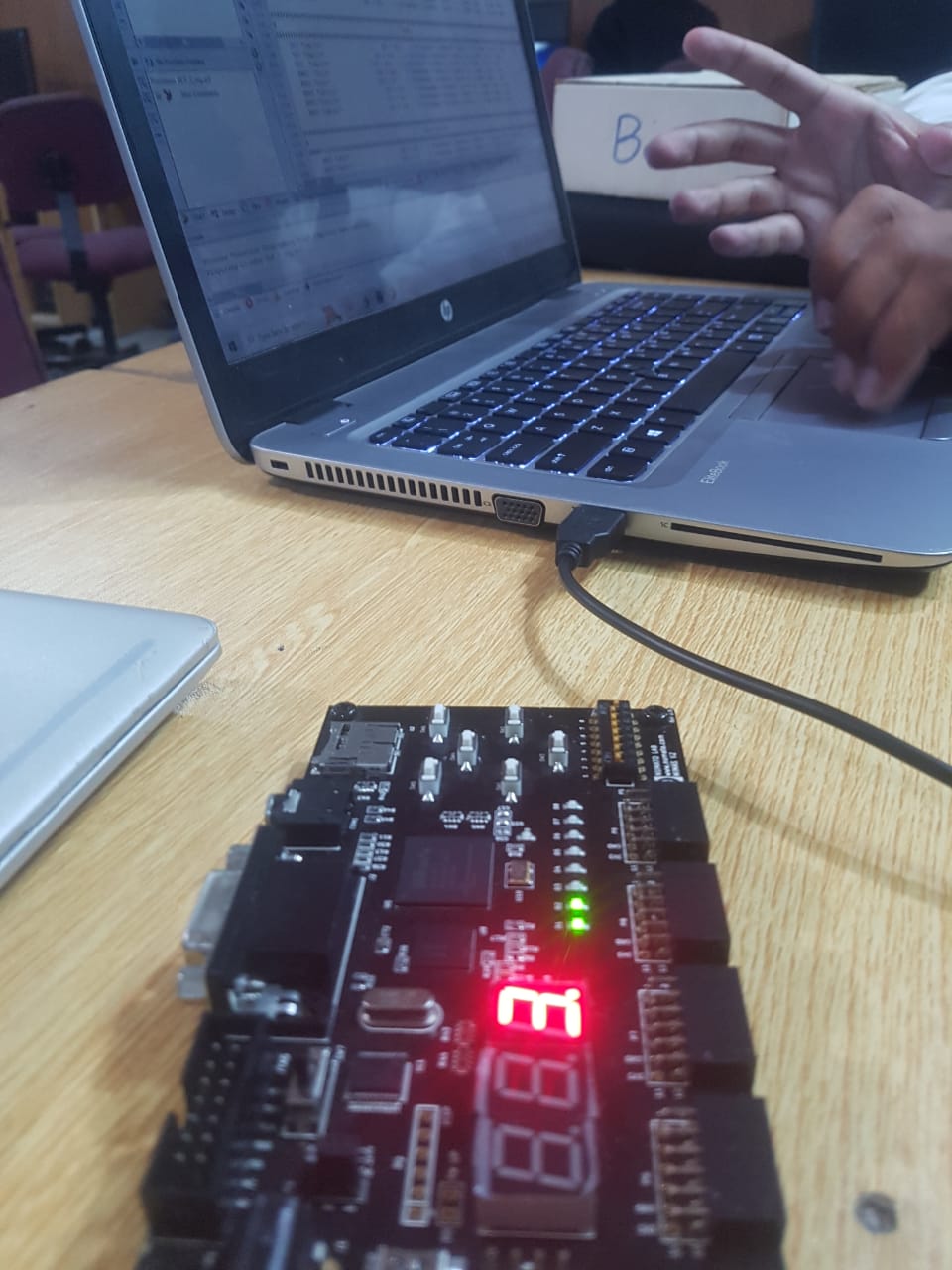
TOP

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UCF:

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FPGA:

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